REMARKS

The Office Action dated November 1, 2005, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

Claims 1, 7 and 8 have been amended. The Applicant submits that the amendments made herein are fully supported in the specification and the drawings as originally filed, and therefore no new matter has been added. Accordingly, claims 1-15 are pending in the present application, and claims 1, 7 and 8 are respectfully submitted for consideration.

Entry of this Amendment is proper under 37 C.F.R. § 1.116 since this Amendment: (a) places the application in condition for allowance for reasons discussed herein; (b) does not raise any new issue regarding further search and/or consideration since the Amendment amplifies issues previously discussed throughout prosecution; (c) does not present any additional claims without canceling a corresponding number of finally-rejected claims and (d) places the application in better form for appeal, should an appeal be necessary. The Amendment is necessary because it is made in reply to arguments raised in the rejection. Entry of the Amendment is thus respectfully requested.

Examiner Interview

The Applicant appreciates the scheduled interview on January 11, 2006.

Allowable Subject Matter

Furthermore, the Applicant appreciates the allowance of claims 5, 6 and 9-15, as well as the indication of allowable subject matter recited in claims 2-4.

Rejection of Claims 1, 7 and 8

Claim 1 was rejected under 35 U.S.C. § 102(e) as being anticipated by Green et al. (U.S. Patent No. 6,496,881, hereinafter "Green"). In addition, claims 7 and 8 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Green. These rejections are respectfully traversed.

Claim 1, as amended recites an information processing apparatus comprising, among other features, a processor connected to a system bus for processing a program stored in a program memory and for generating a pulse signal, a power control circuit coupled to the processor for supplying power to the information processing apparatus when the pulse signal is generated; a stopping means for stopping the power control circuit from supplying the power to the information processing apparatus when the detecting means detects an error of the processor and when the processor stops generating the pulse signal, wherein the information processing apparatus goes into an off-state without depending on a timer.

Claim 7, as amended recites a home-use game device comprising, among other features, a processor connected to a system bus for processing a game program stored in a program memory and for generating a pulse signal, a power control circuit coupled to the processor for supplying power to the home-use game device when the pulse signal is generated; a stopping means for stopping the power control circuit from

supplying the power to the home-use game device when the detecting means detects an error of the processor and when the processor stops generating the pulse signal, wherein the home-use game device goes into an off-state without depending on a timer.

Claim 8, as amended recites a home-use karaoke device comprising, among other features, a processor connected to a system bus for processing a game program stored in a program memory and for generating a pulse signal, a power control circuit coupled to the processor for supplying power to the home-use karaoke device when the pulse signal is generated; a stopping means for stopping the power control circuit from supplying the power to the home-use karaoke device when the detecting means detects an error of the processor and when the processor stops generating the pulse signal, wherein the home-use karaoke device goes into an off-state without depending on a timer.

It is respectfully submitted that the prior art fails to disclose or suggest at least the above-mentioned features of the Applicant's invention.

Green merely discloses processors 31-38 coupled to a memory controller 50 via a bus, where the processors 31-34 communicate with the memory controller 50 via a bus 52, and the processors 35-38 communicate with the memory controller 50 via a bus 54.

The computer 30 of Green includes,

> control logic 64 that can disable one or more of the processors 31-38 during the power up sequence in response to a processor failure. If one of the processors 31-38 is determined to have failed in some respect, the failed processor can be identified, it can be removed from the

continued operation of the computer 30 without disrupting the operation of the other processors so that it may be subsequently removed from the computer or replaced, and/or the user or administrator of the computer 30 can be notified of the processor failure.

...the computer 30 includes a timer 71 associated with and operatively coupled to the processors 31-38 via a bus 80. The timer 71 may be part of the control logic 64. The control logic 64, in turn, is coupled to each of the VRMs 41-48 via a bus 81. If the designated boot processor is operating correctly, it delivers a signal to the timer 71 via the bus 80 to stop the timer 71. However, if the designated boot processor is not operating correctly, the timer 71 times out and the control logic 64 receives a signal from the timer 71 indicating that the designated boot processor 31-38 has failed to boot the computer 30. In response, the control logic 64 disables the VRM associated with that processor to render the processor inoperable.

During a power up sequence, one of the processors 31-38 is initially designated as the boot processor. The processor 31 is initially designated as the boot processor at the time of the initial system reset. (Block 84). At this time, the timer 71 begins counting, and the boot processor attempts to boot the computer 30. If the boot processor 31 is operating correctly, it stops the timer 71 before it times out, and it boots the computer normally. (Blocks 86 and 88). However, if the boot processor 31 fails to boot the computer 30 before the timer 71 times out, the timer 71 delivers a signal to the control logic 64. In response to the signal from the timer 71, the control logic 64 delivers a signal on the bus 81 to the VRM 41 associated with the processor 31 to disconnect the processor's supply voltage delivered by the VRM 41, thus disabling the processor 31. (Block 90). Then, the system resets and another boot processor is assigned from the remaining operable processors 32-38. (Blocks 92 and 94). This process repeats until an operable processor is able to boot the computer 30. (Blocks 86-94).

Column 5, lines 20-54 of Green. Thus, it is submitted that Green provides a system where the power supply to the boot processor is stopped and the computer is reset only when the timer 70 is NOT reset with a predetermined time.

In contrast, one exemplary embodiment of the present invention provides an apparatus or a device where the power supply to the apparatus or device is stopped when an error is detected in the processor and when the processor stops generating a pulse signal, without relying a time function. The processor is connected for processing a program stored in a program memory and for generating the pulse signal. In addition, the present invention includes a power control circuit coupled to the processor for supplying power to the information processing apparatus when the pulse signal is generated, and a stopping means for stopping the power control circuit from supplying the power to the information processing apparatus when the detecting means detects an error of the processor and when the processor stops generating the pulse signal. When the power supply is stopped, the apparatus or the device goes into an off-state without depending on a timer function.

The Applicant further submits that one advantage of the present invention is that it prevents the problem of destroying the contents/data stored in memory when a processor processing a program detects or has an error. It is further submitted that the present invention is capable of preventing data destruction by shutting down the power of the system when an error is detected.

In view of the above, the Applicant submits that Green fails to disclose each and every element recited in claims 1, 7 and 8 of the present application.

Moreover, to qualify as prior art under 35 U.S.C. §102, a single prior art reference must teach, i.e., identically describe, each feature of a rejected claim. As explained above, Green fails to disclose or suggest each and every feature of claims 1, 7 and 8. Accordingly, Applicant respectfully submits that claims 1, 7 and 8 are not anticipated by Green. Therefore, Applicant respectfully submits that claims 1, 7 and 8 are allowable.

Also, it is submitted that in order to establish a *prima facie* case of obviousness, each feature of a rejected claim must be taught or suggested by the applied art of record. See M.P.E.P. §2143.03 and *In re Royka*, 490 F.2d 981 (CCPA 1974). As explained above, Green taken alone does not teach or suggest each feature recited by pending Claims 1, 7 and 8. Accordingly, Applicant respectfully submits that pending Claims 1, 7 and 8 are not rendered obvious under 35 U.S.C. § 103 by Green.

Hence, Applicant respectfully requests withdrawal of the rejections.

Conclusion

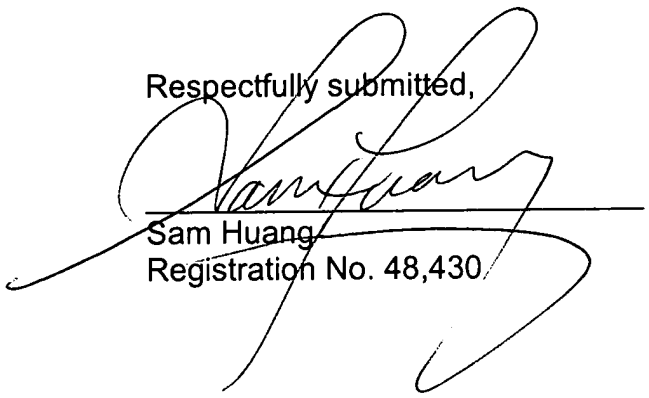
In view of the above, Applicant respectfully submits that each of claims 1, 7 and 8 recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicant also submits that the subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore respectfully requests that claims 1-4, 7 and 8 be found allowable and that this application be passed to issue along with allowed claims 5-6 and 9-15.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the

Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, referring to client-matter number 100341-00016.

Respectfully submitted,



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